Docket No. 500-004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellant:	Chieng-Chung Chen	
Serial No.:	10/696,525	Examiner: Phan, Trong Q
Confirmation No:	6390	Group Art Unit: 2827
Filing Date:	October 29, 2003	
Title:	MEMORY PUMPING CIRCUIT	

MAIL STOP APPEAL BRIEF – PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

APPEAL BRIEF

Appellant submits this Appeal Brief to the Board of Patent Appeals and Interferences on appeal from the decision of the Examiner of Group Art unit 2827 dated December 11, 2006, finally rejecting claims 1, 7-9 and 12-13. The fee of $500 for filing this brief under 37 CFR 41.20(b)(2) is enclosed herewith.

TABLE OF CONTENTS

I) REAL PARTY IN INTEREST

The real party in interest is Winbond Electronics Corp., located in Hsinchu, Taiwan, which is the assignee of this patent application.

II) RELATED APPEALS AND INTERFERENCES

The Appellant knows of no related appeals or interferences that might directly effect or be directly effected by or have bearing on the Board's decision in the pending appeal.

III) STATUS OF CLAIMS

All pending claims 1, 7-9 and 12-13 have been finally rejected and are subject to the present appeal. Former claims 2-6 and 10-11 were previously cancelled.

IV) STATUS OF AMENDMENTS

An amendment (see appendix) after the final office action filed on February 23, 2007, has not been entered (note advisory action of March 6, 2007).

V) SUMMARY OF CLAIMED SUBJECT MATTER

Appellant's claimed invention is directed to a pumping circuit (for example, the first embodiment is best depicted in Fig. 2(A), and the second embodiment is best depicted in Fig. 2(B)), which comprises a DRAM cell (21), a current source (11), and a driving circuit (13 or 22). The DRAM cell (21) is used as a charging capacitor of the pumping circuit, and includes a MOS transistor (211) and a storage capacitor (212). The DRAM cell (21) and the current source (11) are connected at a node (V_{PP}), which provides a pumping voltage (V_{PP}) as a voltage source to a memory device's word line. Specifically, in the arrangement of the DRAM cell (21), the MOS transistor (211) has a source, a drain, and a gate connected together to the node (V_{PP}) and to one plate of the storage capacitor (212). Another plate of the storage capacitor (212) is connected to receive the clock signal θ_2 or α of the driving circuit (13 or 22). One primary advantage of the claimed invention, compared to the appellant's Fig. 1 Prior art or other conventional pumping circuit, is the reduced area of the charging capacitor/DRAM cell (21) required to make sure the driving current is enough for the pumping voltage (V_{PP}).

VI) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1, 7, 9 and 12 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Figure 1 Prior Art, in view of Liu (USP 5,796,670), and Countryman, Jr., (USP 4,532,611).

Claims 8 and 13 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Figure 1 Prior Art, in view of Liu (USP 5,796,670), Countryman, Jr. (USP 4,532,611), and further in view of Hiratsuka et al. (USP 5,453,707).

VII) ARGUMENT

The Prior Art

Appellant's Fig. 1 Prior art

Appellant's Fig. 1 prior art is directed to a pumping circuit, which comprises a current source (11) and a charging capacitor/MOS capacitor (12), connected to provide a pumping voltage (V_{PP}) used as a voltage source for the memory's word line. One primary disadvantage of this prior art pumping circuit is the large area of the charging capacitor/MOS capacitor (12) required to make sure the driving current is enough for the pumping voltage (V_{PP}).

Liu (US Patent 5,796,670)

Liu is directed to a memory cell (for example, 30 in FIG. 3), which comprises a select transistor (12) and capacitors (22/32). In Liu's memory cell (30), one of the source/drain (18) is connected to bitline (V_{BIT}) and another of the drain/source (20) is connected to the capacitor (22).

Countryman (US Patent 4,532,611)

Countryman is directed to a fusible link or switch (for example, 34 in FIG. 5), through which a defective row of memory cells could be replaced with a redundant row of memory cells. In Countryman's fusible link, two ends of the transistor (36) are open when the fusible link is programmed, and the two ends of the transistor (36) provide a current path when the fusible link is unprogrammed (column 5, lines 27-42). The Countryman's fusible link comprises, among others, a programming transistor (37), which has a gate connected to V_{PP}, and source/drain connected to a load transistor (38) and to a select transistor (39). In Countryman's fusible link, the gate and the source/drain are communicated to each other by way of a load transistor (38).

Hiratsuka (US Patent 5,453,707)

Hiratsuka is directed to a clock generation circuit, which (Fig. 4) includes a clock driver (18) consisted of an NMOS transistor Mn1 and a PMOS transistor Mp1, for generating clock signalψ1.

Issues

The Examiner's primary rationale for rejecting Claims 1, 7-9 and 12-13 as being unpatentable over appellant's Fig. 1 prior art, in view of Liu and Countryman, or/and further in view of Hiratsuka was stated as follows in the final office action and again in the advisory action:

Appellant Fig. 1 prior art's NMOS capacitor (12, Fig. 1) could be modified and replaced by Liu's series-connected capacitors (22 and 32, Fig. 3), of which the Liu's capacitor 32 could be successively further modified and replaced by Countryman's transistor (37, Fig. 5) having a source, a drain and a gate connected together.

Appellant believes that the Examiner's rejection was erroneous. The issues regarding the rejection can be succinctly stated as follows:

Issue 1—Whether Claims 1, 7, 9 and 12 are patentable under 35 USC 103 over appellant's Fig. 1 prior art, in view of Liu and Countryman?
Issue 2—Whether Claims 8 and 13 are patentable under 35 USC 103 over appellant's Fig. 1 prior art, in view of Liu and Countryman and further in view of Hiratsuka?
Issue 3—Whether Claim 8 is objected to?

Grouping of Claims

Claims 1, 7-9 and 12-13 stand or fall together.

The Argument

Prior to discussing each issue, appellant would like to bring to the Board's attention the claim amendments made after the final office action but before the advisory action, which were not entered. Examiner asserts in the advisory action that the new feature, (particularly "the MOS transistor has a source, a drain, and a gate connected together") added to Claims 1 and 9 raises new issue that would require further

consideration and/or search. Appellant disagrees with Examiner's assertion on the basis that Examiner has already considered such feature, for example, in the final office action. In the paragraph 3 of the final office action, Examiner has considered and asserts that "Countryman … discloses … transistor 37 having source, drain and gate connected together." It is thus respectfully submitted that all claims currently presented have been well considered by Examiner, and should be entitled to entry for the appeal.

Issue 1—Whether Claims 1, 7, 9 and 12 Are Patentable Under 35 USC 103 Over Appellant's Fig. 1 Prior Art, in View of Liu and Countryman?

The independent Claims 1 and 9, and dependent Claims 7 and 12 are patentable over appellant's Fig. 1 prior art, in view of Liu and Countryman at least on five grounds as follows.

Firstly, appellant's Fig. 1 prior art is directed to a pumping circuit, whereas Liu is directed to a memory cell. Appellant respectfully notes that "pumping circuit" and "memory cell" are two distinct subjects with respective and different technical disciplines. Even the claimed pumping circuit is used in a memory device, as in the embodiment, to provide voltage to a word line of the memory device, the claimed pumping circuit still is not the equivalent of or similar to the memory cell. Accordingly, a person skilled in the pertinent art would not modify appellant's prior art by Liu without hindsight. Specifically, skilled artisan would not utilize the capacitors (22/32 in Fig. 3) of Liu's "memory cell" to replace appellant prior art's charging capacitor (12 in Fig. 1) of the "pumping circuit" at the time of the invention.

For similar reasons, Countryman is directed to a fusible link, which is a subject with technical discipline dramatically different from that of appellant's prior art, and different from that of Liu. Accordingly, a person skilled in the pertinent art would not modify appellant's prior art by Countryman or/and Liu without hindsight. Specifically, skilled artisan would not utilize the transistor (37 in FIG. 5) of Countryman's "fusible link" to replace the transistor (12 in FIG. 3) of Liu's "memory cell," or to replace appellant prior art's charging capacitor (12 in Fig. 1) of the "pumping circuit" at the time of the invention.

Secondly, as asserted in paragraph 3 of the final office action, Examiner alleges it would be obvious to one of ordinary skill in the art to utilize Liu's memory cell in place of appellant prior art's charging capacitor "for the purpose of providing high data storage capacity and low power consumption." Appellant respectfully submits that Examiner's such assertion lacks basis of evidence, and thus there is no incentive to modify appellant's prior art by Liu. Specifically, the whole disclosure of appellant prior art, explicitly or implicitly, has nothing to do with "data storage capacity" or with "power consumption." While Liu is for the purpose of providing high data storage capacity and low power consumption, appellant's prior art, nevertheless, is exclusively directed to the "pumping circuit" for increasing capacitance of the capacitor of the "pumping circuit" (but not of the memory cell). Appellant sees no association between Liu's high data storage capacity/low power consumption in a memory cell with appellant prior art's increasing capacitance in a pumping circuit. Accordingly, appellant respectfully submits that there is no incentive to modify appellant's prior art by Liu.

Thirdly, appellant respectfully submits that purpose or technical principle will be defeated if Liu's memory cell (30 in FIG. 3) is in place of appellant prior art's charging capacitor (12 in Fig. 1) in reaching the claimed invention. Specifically, Liu's memory cell (30 in FIG. 3) has three terminals—one source/drain (18) coupled to a bitline, a gate (16) connected to a word line, and another plate of the capacitor (32) connected to V_{REF}, which is a DC voltage source (column 7, lines 33-37). To the contrast, appellant prior art's charging capacitor (12 in Fig. 1) has two terminals—one terminal connected to provide word line pumping voltage (V_{PP}), and another terminal connected to receive clock signal, which is a non-DC signal source. A person skilled in the art would not know how to replace a two-terminal charging capacitor with a three-terminal memory cell, let along the disparate functions of these terminals. Further, (Liu's) V_{REF} is a DC voltage source, whereas the (appellant's prior art) clock signal is a non-DC signal source. Accordingly, purpose or technical principle will be defeated if appellant's prior art is modified by Liu. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) Further, if the proposed modification or combination of the prior

art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)

Fourthly, appellant disagrees with Examiner's assertion that it would be obvious to utilize Countryman's transistor (37, Fir. 5) in place of Liu's transistor (12), thereby obtaining the claimed invention. This assertion is respectfully traversed on the following reason. Countryman's transistor (37) has its one end connected to V_{PP}, while another end connected to a transistor (39) that receives control signal S. To the contrary, the claimed invention's MOS transistor (211, for example) has its source, drain, and gate connected together to the node (V_{PP}), while also connected to transfer charge to/from the storage capacitor (212, for example). As the Countryman's transistor (37) is disparate from the Liu's transistor (12) (or the claimed invention's MOS transistor) with respect to their functions and with respect to their connections, it too speculative a leap to conclude that Countryman's transistor (37) could be utilized to modify Liu, and that such modification would result in the claimed invention.

Finally, Examiner contends in the final office action and again in the advisory action, that Countryman discloses a transistor (37, Fig. 5) having a source, a drain, and a gate connected together. It is evident through observing Countryman's Fig. 5 that the transistor (37) does not have its source, drain, and gate connected together, as claimed. It is well known to a skilled person that source, drain, and gate connected together means, in its ordinary meaning, that the source electrode, the drain electrode, and the gate electrode are "physically" connected, rather than "indirectly" connected. If the Countryman's transistor (37) is construed to have its source, drain, and gate "connected together," the claim limitation would become superfluous; and *all* electronic devices and their terminals in any circuit would be construed as being "connected together." In summary, a person skilled in the pertinent art or even in the electrical engineering in general, will not consider Countryman's transistor (37) as having its source, drain, and gate "connected together."

For the foregoing reasons, Claims 1, 7, 9 and 12 are considered allowable over the prior art references.

Issue 2—Whether Claims 8 and 13 Are Patentable Under 35 USC 103 Over Appellant's Fig. 1 Prior Art, in View of Liu and Countryman and Further in View of Hiratsuka?

The dependent Claims 8 and 13 are patentable over appellant's Fig. 1 prior art, in view of Liu and Countryman and further in view of Hiratsuka for the same reasons advanced under Issue 1.

Further, even if Hiratsuka discloses a specific driving circuit, Hiratsuka still does not make up the deficiency of the appellant's prior art modified by Liu/Countryman (if the modification is possible).

Claims 8 and 13 are therefore considered allowable over the prior art references.

Issue 3—Whether Claim 8 Is Objected to?

Claim 8 is objected to because of being dependent on a cancelled Claim 6. Appellant accordingly has amended Claim 8, after the final office action but before the advisory action, as now being dependent on Claim 1. As indicated in the advisory action, this amendment, among other amendments, was not entered.

The amendment to Claim 8 is believed to overcome the objection.

CONCLUSION

In light of the above reasons, appellant respectfully submits that Claims 1, 7-9 and 12-13 on appeal are patentable because:

1. appellant's prior art, Liu, and Countryman are individually directed to distinct subjects,

2. there is no incentive to modify appellant's prior art by Liu because of no purpose association therebetween,

3. modifying appellant's prior art by Liu would render the prior art invention being modified unsatisfactory for its intended purpose, or change the principle of operation of the prior art invention,

4. Liu cannot be modified by Countryman because of their disparate functions and connections, and

5. the Countryman's transistor does not have its source, drain, and gate connected together.

If the Board agrees with any one of the statements submitted above, they should allow all the claims on appeal.

Accordingly, the reversal of the Examiner by the honorable Board of Appeals is respectfully solicited.

Respectfully submitted,

/arbarkume/

Date: May 23, 2007

Anthony R. Barkume
Reg. No. 33,831
Attorney for Appellant

20 Gateway Lane
Manorville, NY 11949
tel (631) 259-9099
fax (631) 980-7997

VIII) CLAIMS APPENDIX

(with markings showing the proposed amendments made after the final office action but before the advisory action)

Claim 1. A memory pumping circuit comprising:

a DRAM cell used as a charging capacitor of the memory pumping circuit for enhancing the capacitance, wherein the DRAM cell comprising a MOS transistor and a storage capacitor;

a current source coupled to the DRAM cell for providing a charge current to the DRAM cell;

a node located between the current source and the DRAM cell for providing a pumping voltage used as a voltage source of a word line, and

a driving circuit for generating a clock signal to drive the DRAM cell;

wherein the MOS transistor has a source, a drain, and a gate connected together to the node and to one plate of the storage capacitor, and

wherein another plate of the storage capacitor is connected to receive the clock signal of the driving circuit.

Claim 7. The memory pumping circuit according to Claim 1, wherein said driving circuit is an inverter.

Claim 8. The memory pumping circuit according to Claim [[6]] 1, wherein the driving circuit comprises a PMOS transistor and a NMOS transistor, and generates the clock signal according to a first clock signal and a second clock signal.

Claim 9. A memory pumping circuit comprises:

a current source for providing a charge current;

a DRAM cell as a charging capacitor of the pumping circuit, the DRAM cell having an output port for providing a pumping voltage used as a voltage source of a word line, the output port coupled to the current source for receiving the charge current, wherein the DRAM cell comprising a MOS transistor and a storage capacitor; and

a driving circuit for generating a first clock signal to the DRAM cell for driving the DRAM cell;

wherein the MOS transistor has a source, a drain, and a gate connected together to the output port of the DRAM cell and to one plate of the storage capacitor, and

wherein another plate of the storage capacitor is connected to receive the first clock signal of the driving circuit.

Claim 12. The memory pumping circuit according to Claim 9 wherein the driving circuit is an inverter.

Claim 13. The memory pumping circuit according to Claim 9 wherein the driving circuit comprises a PMOS transistor and a NMOS transistor, and generates the first clock signal according to a second clock signal and a third clock signal.

IX) EVIDENCE APPENDIX

None.

X) RELATED PROCEEDINGS APPENDIX

None.